REMARKS

Applicant thanks the Examiner for considering the reference cited with the Information Disclosure Statement filed February 20, 2003.

Status of the Application

Claims 1-22 are all the claims pending in the Application, as claims 21 and 22 are hereby added. Claims 1-20 have been rejected.

This Action Is Improperly Made "Final"

Applicant respectfully submits that this Action is improperly "Final" for *at least* the reasons indicated in Applicant's Petition to Withdraw Finality, dated June 19, 2003. Specifically, MPEP § 706.07(a) indicates that a "second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) ..." (emphasis added).

Here, the Examiner has introduced new grounds of rejection, *i.e.,* claim 1 as being alternatively anticipated by JP 10-56093 or US 6,018,462, and claim 7 as being anticipated by JP 10-56093. These new rejections were not necessitated by applicant's amendment, as claim 1 was not amended in response to the August 21, 2002 First Office Action, and claim 7 was only amended to correct an informality. Nor were these new rejections based upon information

submitted in an information disclosure statement (IDS) during the 37 C.F.R. § 1.97(c) period[1], as US 6,018,462 was cited by the *Examiner* in the August 21, 2002 Office Action, and JP 10-56093 was provided to the Examiner via an IDS filed with the Application on November 22, 1999, which was long before the required period.

Thus, Applicant respectfully submits that this is an improper "Final" Office Action, and requests the corresponding withdrawal of the "Finality."

Indefiniteness Rejection of Claims 15 and 16 Under 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 15 and 16 as being indefinite under 35 U.S.C. § 112, second paragraph. The Examiner has indicated that there is insufficient literal antecedent basis for the term "said group" in these claims (see Office Action, pg. 2). Applicant has corrected the cited informality in claim 16. However, claim 15 does not recite "said group," and thus the Examiner's rejection is not understood relative to this claim. Thus, withdrawal of this rejection is respectfully requested.

The Examiner's Indication That The Changes Made To 35 U.S.C. § 102(e) By The AIPA Do Not Apply To This Application Is Incorrect

The Examiner has indicated that "the changes made to 35 U.S.C. § 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this Application as the application being examined was not (1) filed on or after November 29, 2000." (Office Action, pg. 3, first full par.). The Examiner is incorrect.

[1] *i.e.*, between the August 21, 2002 first Office Action and the instant Office Action.

The instant Application is based upon a Continued Prosecution Application (CPA) filed on June 24, 2002, which is after November 29, 2000. Thus, the changes made to 35 U.S.C. § 102(e) and 35 U.S.C. § 103(c) by the AIPA are applicable to this Application. (See MPEP § 706.02(l)).

Accordingly, *at least* one reference cited and applied by the Examiner, Sakuyama (US 6,018,462), is not available as prior art to this Application by operation of 35 U.S.C. § 103(c), *at least* when used in a rejection based upon 35 U.S.C. § 103(a). Applicant confirms that both the instant Application and Sakuyama (US 6,018,462) were, at the time the invention of the instant Application was made, owned by NEC Corporation.

Thus, at least the 35 U.S.C. § 103(a) rejections of claims 13-18 which utilize Sakuyama are invalid, and must be withdrawn.

Anticipation Rejections of Claims 1, 7, 14, 15 and 17-20 Under 35 U.S.C. § 102(a)

The Examiner has rejected claims 1, 7, 14, 15 and 17-20 under 35 U.S.C. § 102(a) as being anticipated by JP 10-56093 to Arata et al. (cited by the Examiner as "Kaneshiro"; referred to hereinafter as "JP '093"). This rejection is respectfully traversed.

As an initial matter, Applicant notes that JP '093 was first provided to the Examiner via an IDS filed November 22, 1999. The Examiner indicated that JP '093 was considered on September 6, 2001. However, the Examiner has waited until the instant Office Action (dated May 20, 2003), which is the *fourth* Action on the merits, to utilize JP '093 in an anticipatory rejection of the independent claims. It is difficult to understand the Examiner's delay in applying what he alleges to be an anticipatory reference, especially considering that most of the rejections

in the three previous Office Actions were based upon alleged obvious combinations of references.

Turning towards the reference itself, JP '093 discloses a Ball Grid Array (BGA) semiconductor device 2 connected to a mounting substrate 20. Each external electrode 10 on device 2 is connected to a single land 21 via a solder ball 9. Each solder ball 9 is of the same size. Thus, Applicant respectfully submits that JP '093 is similar to, and no more relevant to the independent claims than, the prior art of the Application (see FIG. 1).

Nevertheless, the Examiner alleges that JP '093 discloses all of the features of independent claims 1, 17 and 19, and takes the following curious (and contradictory) position in the paragraph bridging pages 5 and 6 of the instant Office Action:

> 1. To further clarify the teaching of the limitations, "for a single first solder bump which is larger than second solder bumps for said electrodes arranged other than in said groups of electrodes," and, "so as to be connected to a first solder bump, wherein said first solder bump has a larger lateral cross section than said second solder bump," it is noted that these limitations are statements of intended use of the product which does not result in a structural difference between the claimed product and the product of [JP '093]. Further, because the product of [JP '093] has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of [JP '093]. Similarly, the manner in which a product operates is not germane to the issue of patentability of the product ... Also, expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability.

Thus, at least according to Applicant's understanding, the Examiner seems to be taking the position that the "first solder bumps" recited in independent claims 1, 7 and 19 are not

structural features of the invention, but rather are somehow statements of how the recited electronic part (or assembly) operates.

Applicant respectfully submits that such a position is completely unreasonable based on the clear language of the claims and the Examiner's interpretation of those claims throughout the prosecution of this Application. Further, the very cases the Examiner cites to support his position are inapposite to his conclusion.

First, Applicant notes that, "when not defined by applicant in the specification, the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art." (See MPEP § 2111.01). Applicant assumes the Examiner to be one of ordinary skill in the art. The Examiner originally (and continually) construed claims 1 and 7 to require "solder bumps." Specifically, in the very first Action on the merits, the Examiner, in rejecting independent claims 1 and 7, cites Higashiguchi et al. (US 5,828,128) as disclosing that "electrodes 24 at portions of the electrode arrangement are provided for a single first solder bump 21 which is larger than second solder bumps 22 for said electrode 25 arranged other than said corner portions." (See September 12, 2001 Office Action, pg. 4, first par.). The Examiner maintained this position in the February 25, 2002 Final Office Action. Further, although the Examiner switched references in the third Action on the merits (dated August 21, 2002), he still specifically cited "first solder bump 174 which is larger than second solder bumps 170, 172" as being disclosed by Geffken (US 5,883,435).

Thus, Applicant respectfully submits that the Examiner has interpreted "solder bumps" as required structural elements of independent claims 1 and 7 throughout the prosecution of the instant Application, and cannot now change his interpretation to "fit" newly applied references.

Further, Applicant respectfully submits that independent claims 1, 7 and 19 each recite and require the structure of a "first solder bump." Claim 1 recites that "said groups of electrodes are provided for a single first solder bump which is larger than second solder bumps," claim 7 recites that the electronic assembly further comprises "solder bumps including first solder bumps connected with said groups of electrodes and said first substrate electrodes," and claim 19 recites "at least two first electrodes positioned on a rear surface of said electronic part so as to be connected to a first solder bump," "wherein said first solder bump has a larger lateral cross section than said second solder bump."

Lastly, Applicant respectfully submits that the specific case law cited by the Examiner fails to support his conclusion. The Examiner's positions that: (1)"statements of intended use" do not result in structural differences[2]; (2) "the manner in which a product operates is not germane to the issue of patentability;[3]" and (3) "expressions relating the apparatus to contents

[2] The Examiner has failed to cite any controlling case law for this proposition.

[3] Citing *Ex parte Wikdahl*, 10 USPQ2d 1546, 1548 (BPAI 1989); *Ex parte McCullough*, 7 USPQ2d 1889, 1891 (BPAI 1988); *In re Finsterwalder*, 168 USPQ 530 (CCPA 1971); and *In re Casey*, 152 USPQ 235, 238 (CCPA 1967).

thereof during an intended operation are of no significance in determining patentability[4]" are simply inapplicable to the rejected claims.

Specifically, claims 1, 7 and 19 recite either a "back electrode electronic part" or an "electronic assembly" that include "solder bumps." In either case, the "intended use" or "operation" of the product is electronic. Applicants concede that a recitation of the electronic function of a part may not patentably distinguish the structure of part from relevant prior art. However, no such electronic function is recited in claims 1, 7 and 19. Rather, the Examiner seems only to be concerned with the structural "solder bumps." It seems clear that the claimed "part" or "assembly" is not *used* to achieve these "solder bumps," and does not *provide* "solder bumps" in its operation.

Thus, Applicant respectfully submits that, based upon the Examiner's interpretation of the independent claims in the three previous Office Actions, the plain meaning of the terms in those claims, and the failure of the Examiner to cite any case law on point, the Examiner's entirely new interpretation of the language of the independent claims is inaccurate and improper.

Further, Applicant respectfully submits that the Examiner has not met his burden to show that each and every feature of the independent claims are disclosed, or even suggested, in JP '093.

Applicant respectfully submits that JP '093 fails to teach many of the features recited in independent claims 1, 7 and 19. For example, JP '093 fails to teach or suggest "a single first

[4] Citing *Ex parte Thibault*, 164 USPQ 666, 667 (BD. App. 1969).

solder bump which is larger than second solder bumps" (as recited in claim 1) or that a "first solder bump has a larger lateral cross section than said second solder bump" (as recited in claim 19). All of the solder bumps 9 disclosed in JP '093 are of the same size.

Similarly, JP '093 fails to teach or suggest "said groups of electrodes are provided for a single first solder bump" (as recited in claim 1), "first solder bumps connected with said groups of electrodes" (as recited in claim 7) and "at least two first electrodes positioned on a rear surface" of the electronic part "so as to be connected to a first solder bump" (as recited in claim 19). Each of the solder bumps 9 disclosed in JP '093 are connected to only a single electrode 10 and land 21.

Accordingly, for *at least* the reasons discussed above, Applicant respectfully requests the withdrawal of this rejection.

Anticipation Rejections of Claims 1, 13-15, 19 and 20 Under 35 U.S.C. § 102(e)

The Examiner has rejected claims 1, 13-15, 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by Sakuyama (US 6,018,462; hereinafter "Sakuyama"). This rejection is respectfully traversed.

As an initial matter, Applicant notes that Sakuyama was cited, but not applied, by the Examiner in the August 21, 2002 Office Action. For a reason that is unclear to Applicant, the Examiner has waited until the instant Office Action (dated May 20, 2003), to utilize Sakuyama in an anticipatory rejection of the independent claims. It is difficult to understand the Examiner's delay in applying what he alleges to be an anticipatory reference, especially

considering that the rejections in the previous office action were primarily based upon obviousness.

Turning towards the reference itself, Sakuyama discloses a ball grid array multi-tip module (see FIG. 1) with a substrate 1, mounting pads 3, 4, bare tips 6a-c, and metallic bumps 8,9. An alternative embodiment is disclosed in col. 3, lines 28-35 (FIG. 6), wherein, for pads which are only connected to wiring, *i.e.,* no bumps, a connecting wire 10 can be laid across divisional pads 4Aa-4Ac.

The Examiner takes the position that Sakuyama discloses all of the features of independent claims 1 and 19, and again repeats his position (discussed in detail above with respect to JP '093) that the various recitations of "solder bumps" in independent claims 1 and 19 are "functional," and not "structural." Applicant again disagrees with the Examiner, for *at least* the reasons discussed above.

Further, Applicant respectfully submits that the Examiner has failed to meet his burden to show that each and every feature of claims 1 and 19 are disclosed, or even suggested, by Sakuyama.

Specifically, Applicant respectfully submits that Sakuyama only discloses solder bumps of the same size on respective sides of substrate 1, *i.e.,* all solder bumps 9 are the same size, and all solder bumps 8 are the same size. Thus, this structure cannot teach or suggest a "second solder bump" and larger "first solder bump" connected to electrodes on the same surface (either a "back surface" or a "rear surface") of "a back electrode electronic part," as recited in independent claims 1 and 19.

Thus, Applicants respectfully request that the Examiner withdraw this rejection.

Obviousness Rejections of Claim 16 Under 35 U.S.C. § 103(a)

The Examiner has rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over JP '093 in view of Sakuyama. This rejection is respectfully traversed.

As discussed above, Sakuyama is hereby removed as a reference by operation of 35 U.S.C. § 103(c). Thus, this rejection is invalid, and Applicant respectfully requests that the Examiner withdraw it.

Anticipation and/or Obviousness Rejections of Claims 1 and 3-6

The Examiner has rejected claims 1 and 3-6 under 35 U.S.C. § 102(e) as being anticipated by Geffken et al. (US 5,883,435, hereinafter "Geffken"), or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Geffken in view of Dockerty et al. (US 5,796,169; hereinafter "Dockerty"). This rejection is respectfully traversed.

Geffken

Geffken discloses a method to fabricate a semiconductor device (see FIGS. 1-7). The device (semiconductor portion 100) consists of dielectric layers 102, 114, 130; wiring 104, 106, 108, 110 and 112; contacts 120, 122, 124, 126, 128; transition layers 160, 162 and 164; and bumps 170, 172, and 174.

Dockerty

Dockerty discloses (see FIGS. 1 and 3) copper contacts 2 of printed circuit board 1 connected via solder balls 11 to device pads 4 of integrated circuit device 3. Structural reinforcement is provided by contact 8 and pad 9, connected via support solder 6.

The Examiner's Position With Respect to Claim 1

With regard to the anticipatory rejection of claim 1, the Examiner has taken the position that Geffken discloses "electrodes 124, 126, 128 arranged for solder bumps 172, 174 on a back surface portion of said electronic part ... wherein said electrodes are arranged in groups of electrodes 126, 128 ... and said groups of electrodes are provided for a single first solder bump 174 which is larger than second solder bumps 170, 172" (see Office Action, pg. 4). Further, the Examiner alleges that in FIG. 7, "the illustrated cross-sectional area of first solder bump 174 is larger than that of second solder bumps 170, 172." (see Office Action, pg. 10, last full par.).

However, as the Examiner concedes that "Geffken does not appear to teach literally that the first solder bump is larger than the second solder bump," the Examiner has alternatively rejected claim 1 using an obviousness standard, and has applied a secondary reference, Dockerty. The Examiner takes the position that Dockerty discloses that "a first solder bump 16 is larger than second solder bumps 11" (see Office Action, pg. 7).

Geffken Does Not Teach Or Suggest All Of The Features Of Claim 1

Applicant respectfully submits that Geffken fails to teach or suggest both that "electrodes arranged for solder bumps on a back surface portion of said electronic part," and that "groups of

electrodes are provided for a single first solder bump which is larger than second solder bumps for said electrodes arranged other than in said groups of electrodes" (as recited in claim 1).

As noted above, the Examiner cites contacts 126 and 128 of Geffken as somehow being equivalent to the recited electrodes arranged "on a back surface portion" of the electronic part, and that those contacts are "arranged for solder bumps" as recited in claim 1.

However, as explained in the August 21, 2002 Amendment, contacts 126 and 128 are clearly disclosed in Geffken as being provided underneath dielectric layer 130 and below transition layer 164. Thus, Applicant respectfully submits that these contacts can only reasonably be construed as internal components of the circuit structure disclosed in Geffken. Such internal components cannot be arranged "on a back surface portion" of the electronic part, nor are "arranged for solder bumps" as recited in claim 1.

In fact, Geffken (*see* col. 5, lines 13-17), clearly discloses that the complete semiconductor device consists of all of the dielectric layers 102, 114, 130. Applicant respectfully submits that transition layers 160, 162 and 164 are the only portions that could reasonably be interpreted as approximating the claimed "electrodes." Such a reasonable interpretation is further supported in the Examiner's own identification of an "electrode" as bonding pad 15 in Dockerty and as land 25 in Higashiguchi et al. (US 5,828,128) in previous Office Actions.

However, such a reasonable interpretation would prevent the Examiner from alleging that Geffken could be an anticipatory reference, as transition layers 160, 162 and 164 only have a

one-to-one relationship with bumps 170, 172 and 174, and therefore cannot teach or suggest that "groups of electrodes are provided for a single first solder bump," as recited in claim 1.

In response to the above explanation (included with the November 20, 2002 Amendment), the Examiner has indicated that "Geffken teaches at least that the electrodes are provided in close proximity with or in a direction or location with respect to a back surface portion of the electronic part; therefore, at least for this reason, Geffken teaches that the electrodes are provided on a back surface portion of the electronic part." (See Office Action, pg. 16, last par.).

Applicant respectfully submits that the Examiner is improperly construing the plain language of claim 1. Claim 1 recites "electrodes arranged for solder bumps on a back surface portion of said electronic part." According to the *Merriam Webster Online Dictionary, 10th Edition* (http://www.m-w.com), "on" is defined (at least to indicate position) as follows:

a) 1 a -- used as a function word to indicate position in contact with and supported by the top surface of <the book is lying on the table>
b) b -- used as a function word to indicate position in or in contact with an outer surface <the fly landed on the ceiling> <I have a cut on my finger> <paint on the wall>
c) c -- used as a function word to indicate position in close proximity with <a village on the sea> <stay on your opponent>
d) d -- used as a function word to indicate direction or location with respect to something <on the south> <the garden is on the side of the house>

Here, the Examiner seems to be relying on minor definitions c) and d), rather than the more commonly used definitions a) and b). To support his application of these definitions, the Examiner has cited *May v. Carriage, Inc.* 7 USPQ2d 1593 (N.D.Ind. 1988), *Bocciarelli v. Huffman* 109 USPQ 385 (CCPA 1956) and *Inverness Medical Switzerland Gmbh v. Warner*

Lambert Co. 64 USPQ2d 1933 (CAFC 2002). However, these cases do not give an instruction on how to construe the term "on" in all instances. Rather, they instruct that the term must be construed broadly, but read in concert with the remaining claim terms (*Bocciarelli*), or with the disclosure of the Application (*Inverness).*

Here, Applicant notes that claim 1 does not merely recite "electrodes arranged on said electronic part." Rather, claim 1 specifies that the electrodes are arranged "on a back surface." Further, claim 1 specifies that the electrodes are "arranged for solder bumps." It seems clear that solder bumps cannot be connected to an electrode unless it is exposed on the rear surface of the electronic part. Thus, the Examiner's reading of claim 1 to include internal components of the circuit structure of Geffken is inapplicable, as an internal arrangement would preclude the ability of the electrode to be "arranged for solder bumps."

Accordingly, in view of the entirety of claim 1 and the Application, Applicant respectfully submits that the Examiner's interpretation of the term "on" in claim 1 is inappropriate, and respectfully submits that Geffken fails to teach or suggest "electrodes arranged for solder bumps on a back surface portion of said electronic part," where "groups of electrodes are provided for a single first solder bump," for *at least* the reasons discussed above.

Further, Applicant respectfully submits that Geffken fails to teach or suggest a "first solder bump which is larger than second solder bumps." The Examiner attempts to show that such a feature is disclosed by Geffken by alleging that, in FIG. 7, "the illustrated cross-sectional area of first solder bump 174 is larger than that of second solder bumps 170, 172." (see Office Action, pg. 10, last full par.).

Applicant respectfully submits that, contrary to the Examiner's argument, it is not clear that solder bump 174 is any larger than solder bumps 170, 172 in FIG. 7 of Geffken. Further, it has long been held that, "[w]hen the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. See *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956, USPQ2d 1487, 1491 (Fed. Cir. 2000); *MPEP* § 2125. Applicant respectfully submits that Geffken is completely silent regarding any dimensions of any of the solder bumps 170, 172 or 174. Thus, the Examiner's position that Geffken discloses a "first solder bump which is larger than second solder bumps" is entirely unsupported by Geffken.

Accordingly, as Geffken fails to teach or suggest at least the features discussed above, Applicant respectfully requests that the Examiner withdraw the anticipation rejection of claim 1.

No Conceivable Combination of Geffken and Dockerty Teaches Or Suggests All Of The Features Of Claim 1

Regarding the Examiner's alternative rejection of claim 1 in view of a combination of Geffken and Dockerty, Applicant respectfully submits that even this combination fails to teach or suggest all of the features recited in independent claim 1.

Specifically, as noted above, Geffken simply fails to teach or suggest any "first solder bump" that connects a "group of electrodes" that are disposed "on a back surface of" the electronic part. Geffken only discloses a single bump 170, 172, and 174 disposed atop each of the transition layers 160, 162 and 164, respectively. As discussed above, transition layers 160,

162 and 164 are the only portions of Geffken that could reasonably be interpreted as being arranged on the back surface of semiconductor 100.

Applicant respectfully submits that Dockerty is no more applicable than Geffken, as it too fails to teach or suggest any "first solder bump" that connects a "group of electrodes" that are disposed "on a back surface of" the electronic part.

Specifically, Dockerty teaches only a one-to-one connection between contacts 8 and pads 9. There is simply no teaching or suggestion of any support solder 6 connecting multiple contacts 8 or pads 9. The various shapes of solder 6 (see FIGS. 3 and 5) correspond to sizes of single contacts 8 and pads 9, which is different from that of contacts 2, pads 4 and solder balls 11.

Accordingly, Applicants respectfully submit that neither Geffken nor Dockerty, nor any conceivable combination of the two, teach or suggest any "electrodes arranged for solder bumps on a back surface portion of said electronic part," where "groups of electrodes are provided for a single first solder bump," as recited in claim 1.

Thus, as the applied references fail to teach or suggest *at least* the features noted above, Applicant respectfully submits that the Examiner has not established *prima facie* obviousness. Thus, Applicant respectfully requests the Examiner to withdraw the rejection of claim 1.

Additionally, Applicants respectfully submit that dependent claims 3-6 (and all of the dependent claims 3-6, 7-18 and 20) are allowable *at least* by virtue of their dependency.

Obviousness Rejections of Claims 2 and 7-12 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 2 and 7-12 under 35 U.S.C. § 103(a) as being unpatentable over Geffken in view of Dockerty et al. (US 5,796,169; hereinafter "Dockerty"). This rejection is respectfully traversed.

Regarding claim 7, Applicants respectfully submit that Geffken and Dockerty are deficient in teaching or suggesting *at least* "electrodes arranged on a back surface portion of said electronic part" and "arranged into groups of electrodes" wherein "solder bumps including first solder bumps [are] connected with said groups of electrodes," for *at least* the reasons discussed above in relation to claim 1.

Thus, Applicant respectfully requests the Examiner to withdraw the rejection of claim 7.

Additionally, Applicants respectfully submit that claims 2 and 8-12 are allowable, *at least* by virtue of their dependency.

Obviousness Rejections of Claims 13-15 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Geffken or Geffken in view of Dockerty in further view of Sakuyama. This rejection is respectfully traversed.

Regarding the first alternative obviousness rejection utilizing only Geffken, the Examiner concedes, in the third full paragraph on page 15 of the Office Action, that:

> 2. the references applied to claim 1 do not appear to explicitly teach wherein said group of electrodes are directly connected to said first solder bump; wherein said electrodes arranged for solder bumps protrude from said electronic part so as to support said solder bumps, and wherein said electrodes arranged for solder bumps are provided on the rearmost surface of said electronic part.

As the Examiner has conceded that Geffken fails to teach or suggest such features, Applicants respectfully submit that the obviousness rejection of claims 13-15 utilizing only Geffken is invalid on its face.

Regarding the second alternative obviousness rejection utilizing a combination of Geffken, Dockerty and Sakuyama, Sakuyama (as discussed above) is hereby removed as a reference under operation of 35 U.S.C. § 103(c). Thus, this alternative rejection is invalid.

Thus, Applicant respectfully requests the Examiner to withdraw this rejection.

Obviousness Rejections of Claims 16-18 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Geffken in view of Dockerty in further view of Sakuyama. This rejection is respectfully traversed.

As discussed above, Sakuyama is hereby removed as a reference under operation of 35 U.S.C. § 103(c). Thus, this rejection is invalid, and Applicant respectfully requests that the Examiner withdraw this rejection.

New Claims

New claims 21 and 22 are hereby added to more fully define the invention. New claims 21 and 22 correspond to claims 1 and 19 currently on file, but utilize different terminology. Claims 21 and 22 are fully supported by this application (see FIGS 2-7), and are believed to be allowable for *at least* the reasons discussed above with respect to claims 1 and 19.

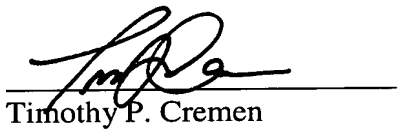
Conclusion

In view of the foregoing, it is respectfully submitted that claims 1-22 are allowable. Thus, it is respectfully submitted that the application now is in condition for allowance with all of the claims 1-22.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees which may be required to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,



Timothy P. Cremen
Registration No. 50,855

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

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